REMARKS

Reconsideration of the present application is respectfully requested. Claims 44, 45, 49, and 63 are pending. No claims have been amended, canceled, or added in the current response.

Summary of Office Action

Claims 44, 45, 49, and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 44, 45, 49 and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 44, 45, 49 and 63 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out distinctly claim the subject matter which applicant regards as the invention.

Claims 44, 45, 49 and 63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent no. 4,766,566 of Chuang ("Chuang") in view of U.S. Patent no. 5,313,331 of Labrousse et al. ("Labrousse"), in view of U.S. Patent no. 4,766,566 of Yokouchi ("Yokouchi"), and further in view of U.S. Patent no. 4,346,437 of Blahut et al ("Blahut").

Discussion of Rejections

Section 112 Rejections

Claims 44, 45, 49, and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Applicants respectfully traverse the rejection.

Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. The examiner must also consider whether the scope of enablement provided to one of ordinary skill in the art by the disclosure is commensurate with the scope of protection sought by the claims. In re Moore, 439 F.2d 1232, 169 USPQ 236 (CCPA 1971). See also MPEP sec. 2164-2164.08.

The Office Action alleged that the limitation from claims 44 and 63, "each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not enabled within the specification upon a cursory glance. The Examiner's attention is respectfully directed to Figure 3 and the related description in the current application.

Figure 3 and its related description in the current application clearly explain and illustrate how each of the at least three functional units has an input coupled directly to one of the at least three dedicated output buses. As set forth in claim 44, the at least three functional units include an arithmetic logic unit (ALU) and a multiplier (claim 44, lines 3-4). For the purpose of illustration, the multiplier and ALU are discussed in details below, with reference to paragraph [0026] and Figure 3 in the specification. As set forth in paragraph [0026], multiplier 23 drives the M-bus 56 using its bus register, M-reg 66; ALU 31 drives the F-bus 55 using its bus register,

F-reg 64 (paragraph [0026], lines 6-7; Figure 3). The M-bus 56 and the F-bus 55 are some examples of the "at least three dedicated output buses." As clearly shown in Figure 3, the ALU 31 (one example of one of the at least three functional units) has an input coupled directly to the M-bus 56 (one example of one of the at least three dedicated output buses). Likewise, the ALU 31 has another input coupled directly to the F-bus 55 (see Figure 3). Therefore, the specification clearly describe "each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" in such a way as to enable one skilled in the art to make and/or use the invention. Withdrawal of the rejection is respectfully requested.

The Office Action further alleged that "[t]he claimed limitation allows for no way of being able to not feedback execution results to the functional units when they are not needed" (Office Action, p. 3, lines 1-2). Although Applicants believe the above allegation has no bearing on the enablement requirement under § 112, first paragraph, Applicants, nevertheless, wish to briefly address this allegation. As is well known in the art, inputs of a functional unit are not necessarily enabled or checked at all times. Therefore, Applicants respectfully traverse the above allegation.

44, 45, 49 and 63 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicants respectfully traverse the rejection.

The Office Action alleged that the limitation from claims 44 and 63, "a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is not contained within the specification upon a cursory glance. Although Applicants previously indicated that written description support for the limitation at issue is found, particularly, in paragraph [0046], Table 1, and the notes at the end of Table 1 in the current application, the

Office Action argued that "Table 1 only shows instructions referencing primarily two ***registers***, ***R and S***" (Office Action, p. 12, lines 1-2; emphasis added). Applicants respectfully disagree with the Office Action for the following reason. Table 1 lists some examples of ALU instructions on the free pipeline assembly code level according to some embodiments of the invention. The notes at the end of Table 1 explicitly state that "***Operand R*** can be selected from busses: A(register), D(data-memory), M(multiplier) and Q(barrel-shifter)" and "***Operand S*** can be selected from busses: B(register), V(image-memory), F(ALU) and U(unary function unit)" (emphasis added). Note that R and S are operands in the instructions, not registers, according to the specification. Further, some of the above buses (such as M(multiplier) and F(ALU)) are dedicated output buses of some functional units (such as multiplier and ALU). By selecting a dedicated output bus of a functional unit as an operand (such as operand R or operand S) in an instruction in Table 1, the instruction explicitly references an individual output of the functional unit. As such, the instructions in Table 1 can explicitly reference individual outputs of any of the functional units. Therefore, the specification of the current application contains written description support for the above limitation.

However, the Office Action asserted that, "[t]o have support for this limitation, the specification ***must say*** that the programmer can explicitly reference ***bypass*** busses in an instruction." (Office Action, p. 12, lines 12-14; emphasis added) The Office Action further argued that:

> The examiner strongly disagrees that one of ordinary skill in the art would find it obvious that the specification in paragraph 46 and figure 3 supports allowing a programmer to directly ***bypass*** operands within instructions without explicit support within the specification. This is especially the case since one of ordinary skill in the art would known [sic] that ***bypassing*** is usually done in hardware and not software. Thus, there's no reason for one of ordinary skill in the art to take away that the ***bypassing*** is done in software by the programmer and not by hardware without explicit support stating that this is the case.

(Office Action, p. 13, lines 1-3; emphasis added)

The claim language at issue does not even include the word, "bypass," and thus, Applicants do not understand why the Examiner insists on the specification to say "bypass" in order to provide support for written description of the limitation of "a second assembly code level which includes ***a plurality of instructions*** which are accessible to the programmer and ***which can explicitly reference individual outputs of any of the plurality of functional units***." Applicants respectfully request the Examiner to further explain the insistence of having the word "bypass" in the specification if the rejection is to be maintained.

The Office Action alleged that the limitation from claims 44 and 63, "each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not contained within the specification upon a cursory glance. Applicants respectfully disagree with the Office Action for the following reason. As explained above, Figure 3 and its related description in the current application clearly explain and illustrate how each of the at least three functional units has an input coupled directly to one of the at least three dedicated output buses. As set forth in claim 44, the at least three functional units include an arithmetic logic unit (ALU) and a multiplier (claim 44, lines 3-4). For the purpose of illustration, the multiplier and ALU are discussed in details below, with reference to paragraph [0026] in the specification. As set forth in paragraph [0026], multiplier 23 drives the M-bus 56 using its bus register, M-reg 66; ALU 31 drives the F-bus 55 using its bus register, F-reg 64 (paragraph [0026], lines 6-7; Figure 3). The M-bus 56 and the F-bus 55 are examples of the "at least three dedicated output buses." As clearly shown in Figure 3, the ALU 31 (an example of one of the at least three functional units) has an input coupled directly to the M-bus 56 (an example of one of the at least three dedicated output buses). Likewise, the ALU 31 has another input coupled

directly to the F-bus 55 (see Figure 3). Therefore, the specification clearly provide support for written description of the limitation of "each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses." Withdrawal of the rejection is respectfully requested.

Claims 45 and 49 are rejected due to their dependency, and thus, the above remarks with respect to claim 44 have overcome the rejection of claims 45 and 49. Withdrawal of the rejection is respectfully requested.

Claims 44, 45, 49, and 63 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully traverse the rejection.

The Office Action states:

> The limitation from claims 44 and 63 "Each [sic] of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses" is not enabled within the specification upon a cursory glance. The specification doesn't detail how the output bus of a function unit can be directly connected to an input of a functional unit. Allowing such a limitation results in a plurality of outputs from functional units fed directly back into the function units regardless of if they are needed for execution or not. The claimed limitation allows for no way of being able to not feedback execution results to the function units when they are not needed.

(Office Action, p. 4, last paragraph)

The test for definiteness under 35 U.S.C. § 112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986); see also MPEP sec. 2173.02. When the limitation at issue is read in light of the specification, in particular, Figure 3 and its related description, one of ordinary skill in the art would understand what is claimed for the reason discussed above. Furthermore, the allegation that the claimed limitation allows for no way of being able to not feedback execution

results to the function units when they are not needed has no bearing on the test for definiteness under current case law and MPEP guidelines. Applicants, nevertheless, wish to briefly address this allegation. As is well known in the art, inputs on a functional unit are not necessarily enabled or checked at all times. Therefore, Applicants respectfully traverse the above allegation.

Prior Art Rejections

Claim 44 recites:

> 44. (Previously presented) A processor comprising:
> at least three functional units coupled to each other to execute operations defined from an instruction set of the processor, the at least three functional units including an arithmetic logic unit (ALU) and a multiplier, the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including
> a RISC/CISC assembly code level,
> a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units, and
> a vector processing assembly code level, using which an individual instruction can be used to cause an operation to be automatically repeated sequentially a programmable number of times on different data words;
> a plurality of control registers, the plurality of hierarchical instruction levels further comprising a fourth level corresponding to the control registers, using which individual instruction words executed by one or more of the functional units can be extended by bits in the control registers on a per-instruction-cycle basis; and
> a bus routing structure that includes **at least three dedicated output buses, including a separate dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses.**
> (Emphasis added.)

The cited references failed to disclose such a processor, particularly one which includes a bus routing structure that includes at least three dedicated output buses, including a separate

dedicated output bus for each of the at least three functional units, each of the at least three dedicated output buses being dedicated to convey data output by a separate one of the at least three functional units, each of the at least three functional units having an input coupled directly to one of the at least three dedicated output buses.

Regarding the above-emphasized limitations, the Examiner appears to rely upon Chuang as disclosing similar limitations in rejecting dependent claims 49 and 50. The Office Action cites Chuang at Figure 7, elements 24, 60, and 70, stating "[e]lements 24, 60, and 70 are three functional units with three separate dedicated output buses to convey output data. These output buses are ***indirectly*** coupled to the inputs of elements 24, 60, and 70 via the output registers, register file, and input registers" (Office Action, p. 6, second paragraph; emphasis added). As clearly set forth in claim 44, "each of the at least three functional units having an input coupled ***directly*** to one of the at least three dedicated output buses" (claim 44, emphasis added). In contrast, the output buses in Chuang are ***indirectly*** coupled to the inputs of the alleged functional units (elements 24, 60, and 70). Therefore, Chuang fails to disclose the above limitation.

Furthermore, none of Labrousse, Yokouchi, and Blahut, alone or in combination, teaches the above limitation. Because Chuang, Labrousse, Yokouchi, and Blahut, alone or in combination, fail to teach the above limitation of claim 44, claim 44 is patentable over Chuang in view of Labrousse, Yokouchi, and Blahut for at least this reason. Withdrawal of the rejection is respectfully requested.

In addition to, or as alternative to, the above reason, claim 44 is patentable over Chuang in view of Labrousse, Yokouchi, and Blahut for the following reason. Claim 44 sets forth "a second ***assembly code level*** which includes ***a plurality of instructions*** which are accessible to the

programmer and ***which can explicitly reference individual outputs of any of the plurality of functional units***." (emphasis added) In contrast, none of Chuang, Labrousse, Yokouchi, and Blahut teaches the above limitation. However, the Office Action alleged that Labrousse discloses the above limitation, citing column 13, lines 35-42 and column 14, lines 17-22 of Labrousse. The Office Action construed Labrousse to disclose instructions that contain bypass encoding signals available to the programmer and implemented into the instructions upon being compiled. (Office Action, p. 6, last paragraph) Applicants respectfully disagree with the Office Action.

According to Labrousse, the bypass signal is for an imitation multiport memory (Labrousse, col. 13, ln. 40-42). Specifically, the bypass signal is for allowing simultaneous read and write to ***an individual memory storage cell*** (such as cell 202 in Figure 6) (Labrousse, Figure 6; col. 12, ln. 29 – col. 13, ln. 34). Labrousse does not teach a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference ***individual outputs of any of the plurality of functional units***.

Furthermore, although Labrousse states that this software controlled bypass technique could also be applied in the register file contained in Register Unit RG if simultaneous write and read access were desired there (Labrousse, col. 14, ln. 17-22), reading Labrousse as a whole, Labrousse merely refers to applying his technique to access individual storage registers within the Register Unit RG, not to explicit reference individual outputs of the functional units.

Moreover, Labrousse explicitly states that the only restriction is that the equality of the port addresses must be known in advance when the instruction words are being ***compiled*** (Labrousse, col. 14, ln. 23-25; emphasis added). It is well known in the art that high-level

programming language instructions are compiled, but not instructions on assembly code level. Therefore, the instructions in Labrousse are ***high-level programming language instructions***, not ***assembly code level***. In other words, Labrousse does not disclose an ***assembly code level*** including instructions which can explicitly reference individual outputs of any of the plurality of functional units.

For at least the above reasons, Labrousse fails to teach the limitation of a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

Furthermore, none of Chuang, Yokouchi, and Blahut, alone or in combination, teaches the above limitation. Because Chuang, Labrousse, Yokouchi, and Blahut, alone or in combination, fail to teach the above limitation of claim 44, claim 44 is patentable over Chuang in view of Labrousse, Yokouchi, and Blahut for at least this reason. Withdrawal of the rejection is respectfully requested.

Claim 63 is patentable over Chuang in view of Labrousse, Yokouchi, and Blahut for at least the reason discussed above with respect to claim 44. Withdrawal of the rejection is respectfully requested.

Dependent Claims

Claims 45 and 49 depend from claim 44, and thus, are patentable over Chuang in view of Labrousse, Yokouchi, and Blahut. Withdrawal of the rejection is respectfully requested.

In view of the above remarks, a specific discussion of the dependent claims is considered to be unnecessary. Therefore, Applicants' silence regarding any dependent claim is not to be interpreted as agreement with, or acquiescence to, the rejection of such claim or as waiving any argument regarding that claim.

Conclusion

For the foregoing reasons, the rejections have been overcome.

Pursuant to 37 C.F.R. §1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: 3/20/08

By: _____
Chui-kiu Teresa Wong
Attorney for Applicants
Reg. No. 48,042

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
(408) 720-8300